Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method of integrating at least one high voltage metal oxide semiconductor (HVMOS) device and at least one Submicron metal oxide semiconductor (Submicron MOS) device on a substrate comprising:

providing the substrate;

forming a plurality of shallow trenches having different depths on a surface of the substrate, the shallow trenches comprising drift shallow trenches and isolation shallow trenches; [[and]]

forming a plurality of silicon oxide layers filling up the shallow trenches, a top of each of the silicon oxide layers being in the shape of a mushroom; and

forming two isolation ion implantation regions underneath the isolation shallow trenches to isolate the high voltage metal oxide semiconductor device and the Submicron metal oxide semiconductor device.

2. (Original) The method of claim 1 wherein a depth of the shallow trenches of the Submicron metal oxide semiconductor device is greater than a depth of the shallow trenches of the high voltage metal oxide semiconductor device.

3. (Canceled)

4. (Original) The method of claim 3 wherein a depth of the isolation shallow trenches is greater than a depth of the drift shallow trenches.

5. (Original) The method of claim 3 wherein two drift ion implantation regions are

formed underneath the drift shallow trenches in an active region of the high voltage metal oxide semiconductor device.

6. (Canceled)

7. (Original) The method of claim 1 wherein to form a plurality of shallow trenches having different depths comprises the following steps:

forming a pad oxide layer on the surface of the substrate;

forming a silicon nitride layer on a surface of the pad oxide layer;

forming a first hard mask patterns on a surface of the silicon nitride layer;

performing a first etching process to remove portions of the silicon nitride layer and the substrate not covered by the first hard mask patterns to form a plurality of shallow trenches of the high voltage metal oxide semiconductor device;

forming a second hard mask patterns on the surface of the silicon nitride layer; and

performing a second etching process to remove portions of the silicon nitride layer and the substrate not covered by the second hard mask patterns to form a plurality of shallow trenches of the Submicron metal oxide semiconductor device.

8. (Original) The method of claim 7 wherein the first hard mask patterns are defined by a first mask produced by tooling database of at least one active region outside the Submicron metal oxide semiconductor device.

9. (Original) The method of claim 7 wherein the second hard mask patterns are defined by a second mask produced by tooling database of at least one active region of the Submicron metal oxide semiconductor device.

10. (Original) The method of claim 7 wherein to form a plurality of silicon oxide layers having the tops in the shape of a mushroom comprises the following steps:

performing an isotropic etching process to remove portions of the silicon nitride layer along an interface of the pad oxide layer and the silicon nitride layer;

forming a silicon oxide layer on the surface of the substrate, and the silicon oxide layer filling up the shallow trenches;

performing a chemical mechanical polishing (CMP) process to remove the silicon oxide layer above a top surface of the silicon nitride layer so that a top surface of the silicon oxide layer is aligned with the top surface of the silicon nitride layer; and

removing the silicon nitride layer.

11. (Original) The method of claim 10 further comprising a step for forming a linear oxide layer in an inner surface of the shallow trenches after performing the isotropic etching process.

12. (Original) The method of claim 10 wherein a thickness of the silicon nitride layer removed by the isotropic etching process is 100 to 300 Å.

13. (Original) The method of claim 10 wherein the silicon oxide layer is formed by performing an atmospheric pressure chemical vapor deposition (APCVD) process.

14. (Original) The method of claim 1 wherein to form the silicon oxide layers having the tops in the shape of a mushroom is to prevent a kink effect.

15. (Currently amended) A method of integrating at least one high voltage metal oxide semiconductor (HVMOS) device and at least one Submicron metal oxide semiconductor (Submicron MOS) device on a substrate comprising:

providing the substrate of a first conductive type;

forming a deep well region of the Submicron metal oxide semiconductor device of a second conductive type;

forming a plurality of shallow trenches having different depths on a surface the substrate, the shallow trenches comprising drift shallow trenches and isolation shallow trenches; [[and]]

forming a plurality of silicon oxide layers filling up the shallow trenches, a top of each of the silicon oxide layers being in the shape of a mushroom; and

forming two isolation ion implantation regions underneath the isolation shallow trenches to isolate the high voltage metal oxide semiconductor device and the Submicron metal oxide semiconductor device.

16. (Original) The method of claim 15 wherein the first conductive type and the second conductive type are opposite to each other.

17. (Original) The method of claim 16 wherein the first conductive type is P type, and the second conductive type is N type.

18. (Original) The method of claim 16 wherein the first conductive type is N type and the second conductive type is P type.

19. (Original) The method of claim 15 wherein a depth of the shallow trenches of the Submicron metal oxide semiconductor device is greater than a depth of the shallow trenches of the high voltage metal oxide semiconductor device.

20. (Canceled)

21. (Original) The method of claim 20 wherein a depth of the isolation shallow trenches is greater than a depth of the drift shallow trenches.

22. (Original) The method of claim 20 wherein two drift ion implantation regions are

formed underneath the drift shallow trenches in an active region of the high voltage metal oxide semiconductor device.

23. (Canceled)

24. (Original) The method of claim 15 wherein to form a plurality of shallow trenches having different depths comprises the following steps:

forming a pad oxide layer on the surface of the substrate;

forming a silicon nitride layer on a surface of the pad oxide layer;

forming a first hard mask patterns on a surface of the silicon nitride layer;

performing a first etching process to remove portions of the silicon nitride layer and the substrate not covered by the first hard mask patterns to form a plurality of shallow trenches of the high voltage metal oxide semiconductor device;

forming a second hard mask patterns on the surface of the silicon nitride layer; and

performing a second etching process to remove portions of the silicon nitride layer and the substrate not covered by the second hard mask patterns to form a plurality of shallow trenches of the Submicron metal oxide semiconductor device.

25. (Original) The method of claim 24 wherein the first hard mask patterns are defined by a first mask produced by tooling database of at least one active region outside the Submicron metal oxide semiconductor device.

26. (Original) The method of claim 24 wherein the second hard mask patterns are defined by a second mask produced by tooling database of at least one active region of the Submicron metal oxide semiconductor device.

27. (Original) The method of claim 24 wherein to form a plurality of silicon oxide layers having the tops in the shape of a mushroom comprises the following steps:

performing an isotropic etching process to remove portions of the silicon nitride layer along an interface of the pad oxide layer and the silicon nitride layer;

forming a silicon oxide layer on the surface of the substrate, and the silicon oxide layer filling up the shallow trenches;

performing a chemical mechanical polishing (CMP) process to remove the silicon oxide layer above a top surface of the silicon nitride layer so that a top surface of the silicon oxide layer is aligned with the top surface of the silicon nitride layer; and

removing the silicon nitride layer.

28. (Original) The method of claim 27 further comprising a step for forming a linear oxide layer in an inner surface of the shallow trenches after performing the isotropic etching process.

29. (Original) The method of claim 27 wherein a thickness of the silicon nitride layer removed by the isotropic etching process is 100 to 300 Å.

30. (Original) The method of claim 27 wherein the silicon oxide layer is formed by performing an atmospheric pressure chemical vapor deposition (APCVD) process.

31. (Original) The method of claim 15 wherein to form the silicon oxide layers having the tops in the shape of a mushroom is to prevent a kink effect.

32. (Original) The method of claim 15 wherein the high voltage metal oxide semiconductor device is operated at +/- high voltage.

33. (Original) The method of claim 15 wherein the deep well region is used to prevent a

back bias effect when the high voltage metal oxide semiconductor device is operated at +/- high voltage.